EEL 308

Minor-1 (2013)

Time: 1 hour **Total: 20**

1. Consider two different implementations - P1 and P2 of the same instruction set. There are five classes of instructions (A, B, C, D and E) in the instruction set. The clock rate and CPI of each class is given below.

Processor	Clock rate	CPI class A	CPI Class B	CPI Class C	CPI Class D	CPI Class E
P1	2 GHZ	1	2	3	4	3
P2	4 GHZ	2	2	2	4	4

If the number of instructions executed in a certain program is divided equally among the classes of instruction except for Class A, which occurs twice as often as each of the others, which computer is faster? How much faster is it? (2)

2. MIPS uses a signed 16-bit value as the branch offset for the PC-relative addressing mode.Is this statement correct? If not, state the statement correctly.

The offset represents byte addresses, what is the branching address range? How could you access a memory location outside this range on a conditional branch?

(1 + 2)

3. Consider the following MIPS code

```
LOOP : slt   $t2, $0, $t1        : set less than
       beq   $t2, $0, DONE
       subi  $t1, $t1, 1
       addi  $s2, $s2 , 2
       j     LOOP
DONE :
```

(i) For the loops above, write the equivalent C (or C like high level language) code routine. Assume that the registers $s1, $s2, $t1, and $t2 are integers A, B, i and temp, respectively.

(ii) For the loop written in MIPS assembly above, assume that the register $t1 is initialized to the value N. How many MIPS instructions are executed? (2 + 1)

4. Consider the following ARM code

```
       MOV   r0, #10      : initialise loop counter to 10
LOOP:  ADD   r0, r1       : add r1 to r0
       SUBS  r0,1         : decrement counter
       BNE   LOOP         : Z=0  repeat loop
```

i. For the ARM assembly code above, write an equivalent MIPS assembly code routine.

ii. What is the total number of ARM assembly instructions required to execute the code? What is the total number of MIPS assembly instructions required to execute the code?

iii. Assuming that the average CPI of the MIPS assembly routine is the same as the average CPI of the ARM assembly routine, and the MIPS processor has an operation frequency that is 1.5 times the ARM processor, how much faster is the ARM processor than the MIPS processor? (3 + 1 + 1)

5. Consider the following code for computation of factorial:

```
FACT: sw    $ra, 4($sp)
      sw    $a0,0($sp)
      addi  $sp, $sp,-8
      slti  $t0,$a0,1
      beq   $t0, $0, L1
      addi  $v0,$0, 1
      addi  $sp,$sp, 8
      jr    $ra
L1    addi  $a0,$a0,-1
      jal   FACT
      addi  $sp,$sp,8
      lw    $a0,0($sp)
      lw    $ra, 4($sp)
      mul   $v0, $a0, $v0
      jr    $ra
```

The integer input is passed through the register $a0 and result is returned in register $v0. Is the above code correct? Verify. If not, identify the error. Correct the code to eliminate the error. (2+2)

6. (i) Consider the following statements in a C-like high level language

A[4,2] = A[4,2]+ 3;

Provide a translation of the above code in the assembly language of 8086 assuming that an integer is stored in 16 bits and A is declared as

int A[10,10]; (2)

(ii) What is the functional role of segment registers in 8086? (1)